

REMARKS

Applicants appreciate the Examiner's attention to the above referenced application. Claims 1-21 were rejected. Claims 1, 2, 15, and 17 have been amended. Claims 1 – 21 are now pending, of which claims 1, 8, 15, and 19 are independent.

Priority

Applicants appreciate the Examiner's acknowledgement of Applicants' claim for foreign priority based on an application filed in Russia on 2/21/2005. Applicants respectfully request clarification of the Examiner's comment that "applicant has not filed a certified copy of the PCT/RU05/D000075 application as required by 35 U.S.C. 119(b)." (See Office Action dated September 29, 2008, page 2.) Applicants have attached a copy of the Notice of Acceptance of the Application mailed by the USPTO on July 1, 2008, indicating that a copy of the international application has been received. Applicants have also attached a copy of the international application for the Examiner's convenience. Applicants respectfully request that any further actions that are necessary by Applicants be explicitly stated in a subsequent Office Action.

35 USC § 101 Rejection of the Claims

Claims 1-7 and 15-18 were rejected under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter. Claims 1, 2, and 15 were amended in response to this rejection and are now believed to be in condition for allowance. Applicants respectfully request that claims 1-7 and 15-18 be allowed to pass to issuance.

35 USC § 102 Rejection of the Claims

Claims 1 – 21 were rejected under 35 USC § 102(b) as being anticipated by Aamodt et al., U.S. Patent Number 6,732,114B1 (hereinafter Aamodt). Applicants respectfully traverse this rejection, which should be withdrawn for at least the reasons set forth herein.

Amended independent claim 1 is repeated below:

1. A method of stable incremental layout of a hierarchical graph comprising:

determining a level of the layout for each new node of the graph using information about hidden nodes of the graph, wherein the determining the level of the layout is performed in a memory associated with a processor;

determining positions of nodes on levels of the layout using information about hidden nodes of the graph, wherein the determining the positions of the nodes is performed in the memory associated with the processor; and

determining coordinates of new nodes in the layout without using information about hidden nodes, wherein the determining the coordinates of the new nodes is performed in the memory associated with the processor.

The Office Action states on page 3 that “determining a level of the layout for each new node of the graph using information about hidden nodes of the graph” is taught by Aamodt in column 9, lines 21-23, and in column 14, lines 47-48. Applicants respectfully disagree. These portions of columns 9 and 14 of Aamodt describe creating a preliminary layout structure for nodes in the graph, and creating an entry in a preliminary layout node array within the preliminary layout structure for the “Current” node if the “Current” node does not already have a row and column identity in a virtual memory grid. (See Aamodt column 14, lines 39-51.) However, Applicants can find no reference to the use of information about hidden nodes of the graph in determining a level of the layout for each new node of the graph. In fact, Applicants respectfully submit that Aamodt teaches away from “determining a level of the layout for each new node of the graph using information about hidden nodes of the graph” in column 9, lines 51-54, where Aadmot states the following: “It is necessary to determine which last visible node precedes the current node, **because hidden nodes that are not displayed cannot be used to position nodes that are displayed** (emphasis added).” If hidden nodes cannot be used to position nodes that are displayed, then no teaching is provided of “determining a level of the layout for each new node of the graph using information about hidden nodes of the graph,” as required by independent claim 1. For at least this reason, independent claim 1 and respective dependent claims 2-9 are allowable.

Independent claims 8, 15, and 19 contain substantially similar limitations that require the use of information about hidden nodes of the graph to determine a level of the layout for other

nodes in the graph. Independent claims 8, 15, and 19, and respective dependent claims 9-14, 16-18, and 20-21 are therefore allowable for at least the foregoing reasons. Applicants respectfully request that claims 1-21 be allowed to pass to issuance.

CONCLUSION

Applicant respectfully requests reconsideration in view of the remarks and amendments set forth above. If the Examiner has any questions, the Examiner is encouraged to contact the undersigned at **512-732-1303**. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0221 and please credit any excess fees to such account.

Respectfully submitted,

Customer Number - 59796

Dated: 1/29/09

/D'Ann Naylor Rifai/
D'Ann Naylor Rifai,
Reg. No. 47,026
Senior Patent Attorney
Intel Corporation
512-732-1303

Intel Corporation
c/o Intellevate, LLC
P.O. Box 52050
Minneapolis, MN 55402